Intelligent signal and data processing for the next generation of new large instruments: study of real time signal flow reduction schemes.

PhD students: Anton Bogachev and Sergei Lapin (1,*)

Supervisors: *Prof. Valeri Saveliev* [1], *Prof. Aurore Savoy-Navarro* [2]

1)Immanuel Kant Baltic Federal University (RU) 2) APC-CNRS/Paris Diderot, Paris (FR)

Modeling of the Front-End ASIC and data transmission in the case of the next generation of Pixel-based devices to be running at the High Luminosity LHC or for highly pixelated instruments

Work is focused on studying different ways to make more compact, i.e. to reduce the amount of data to be sent from the instruments, by using new clustering techniques with as ultimate objective to be translated into the hardware front-end design by the microelectronics team. To do so, will be studied how to improve/optimize the overall data flow architecture of these instruments.